CLAIMS

We claim:

1. A method of extracting electrical characteristics from an integrated circuit layout, said method comprising:

dividing said integrated circuit layout into at least one extraction sub problem;

identifying a set of physical parameters that define said extraction sub problem from said integrated circuit layout;

supplying said set of physical parameters to a machine-learning model trained with Bayesian inference implemented with a Monte Carlo method; and

calculating at least one electrical characteristic for said extraction sub problem by analyzing said set of physical parameters with said machine-learning model trained with Bayesian inference implemented with a Monte Carlo method.

2. The method as claimed in claim 1 wherein said electrical characteristic comprises capacitance.

3. The method as claimed in claim 1 wherein said electrical characteristic comprises resistance.

4. The method as claimed in claim 1 wherein said extraction sub problem comprises a net.

5. The method as claimed in claim 1 wherein said extraction sub problem comprises a section of interconnect wiring.

6. The method as claimed in claim 1 wherein one of said set of physical parameters comprises a distance between a pair of interconnect lines.

7. The method as claimed in claim 1 wherein one of said set of physical parameters comprises a wire width.

8. The method as claimed in claim 1 wherein one of said set of physical parameters comprises a wire length.

9. The method as claimed in claim 1, said method further comprising:

selecting said machine-learning model from a plurality of machine-learning models.

10. The method as claimed in claim 1 wherein calculating at least one electrical characteristic for said extraction sub problem comprises:

determining a capacitance per unit length for a subsection of interconnect wiring; and

multiplying said capacitance per unit length by a length of said subsection of interconnect wiring.

11. A computer readable medium, said computer readable medium comprising an arranged set of computer instructions for:

dividing an integrated circuit layout into at least one extraction sub problem;

identifying a set of physical parameters that define said extraction sub problem from said integrated circuit layout;

supplying said set of physical parameters to a machine-learning model trained with Bayesian inference implemented with a Monte Carlo method; and

calculating at least one electrical characteristic for said extraction sub problem by analyzing said set of physical parameters with said machine-learning model trained with Bayesian inference implemented with a Monte Carlo method.

12. The computer readable medium as claimed in claim 11 wherein said electrical characteristic comprises capacitance.

13. The computer readable medium as claimed in claim 11 wherein said electrical characteristic comprises resistance.

14. The computer readable medium as claimed in claim 11 wherein said extraction sub problem comprises a net.

15. The computer readable medium as claimed in claim 11 wherein said extraction sub problem comprises a section of interconnect wiring.

16. The computer readable medium as claimed in claim 11 wherein one of said set of physical parameters comprises a distance between a pair of interconnect lines.

17. The computer readable medium as claimed in claim 11 wherein one of said set of physical parameters comprises a wire width.

18. The method as claimed in claim 1 wherein one of said set of physical parameters comprises a wire length.

19. The computer readable medium as claimed in claim 11 wherein said arranged set of computer instructions further perform:

selecting said extraction sub problem model from a plurality of extraction sub problem models.

20. The computer readable medium as claimed in claim 11 wherein a subset of computer instructions for calculating at least one electrical characteristic for said extraction sub problem perform the follow:

determining a capacitance per unit length for a subsection of interconnect wiring; and

multiplying said capacitance per unit length by a length of said subsection of interconnect wiring.